IN THE CLAIMS

Please amend the claims as set out in the following claim listing:

1. (Currently Amended) A digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks connected to a common bus, each digital signal processing block including at least a signal processing block for decoding and processing high speed streams of data, each of at least some of said digital signal processing blocks being operative to control hardware associated with said block and having (a) a hardware driver performing a predetermined function assigned to ~~the~~ said block ~~that has the hardware driver~~ for driving the hardware associated with said block and (b) a processing unit for activating said hardware driver to control said associated hardware ~~of particular structure coupled to the block that has said hardware driver to perform said predetermined function~~ in response to a high layer command supplied to said processing unit;

a host processing block for controlling said digital processing apparatus by outputting to the processing unit in a respective digital signal processing block said high layer command, said high layer command being independent of the particular structure of the hardware coupled to said digital processing block, said high layer command being free of those functionality instructions that control individual ones of said predetermined functions of the hardware driver in said respective digital signal processing block, said high layer command being a general-purpose script type command that is interpreted by the processing unit in the digital signal processing block to which said high layer command is supplied to perform the function generally described by said high layer command, and said high layer command not being on a real time basis, said high layer command instructing the processing unit in said digital signal processing block to activate said hardware driver of said digital

signal processing block to perform the predetermined function assigned to said respective digital signal processing block; and

a common bus for connecting said host processing block and said plurality of digital signal processing blocks together for transferring via said common bus both said high layer command that is not on a real time basis and said high speed streams of data,

wherein said processing unit of each of said digital signal processing blocks interprets and executes said high layer command to produce driver control instructions for said hardware driver to operate said hardware of particular structure ~~coupled to~~ associated with said digital signal processing block in accordance with said high layer command.

2. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein said plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast, and

wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware.

3. - 5. (Canceled)

6. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein the high layer command is described and embedded in a script of hypertext,

wherein the hypertext is interpreted by a browser and an indication for operating a function is displayed, and

wherein an instruction corresponding to the function is generated.

7. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein the high speed streams of data contain video data and / or audio data.

8. (Original) The digital signal processing apparatus as set forth in claim 7,

wherein the video data and / or the audio data has been compressed.

9. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein said bus is a general-purpose bus, and

wherein blocks can be added to said bus and a substitute for a connected block can be connected to said bus.

10. (Previously Presented) The digital signal processing apparatus as set forth in claim 9,

wherein when a block is added or substituted, software for operating the added or substituted block is automatically installed.

11. (Original) The digital signal processing apparatus as set forth in claim 9,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

12. (Previously Presented) The digital signal processing apparatus as set forth in claim 9,

wherein when a block is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

13. (Currently Amended) A digital signal processing method, comprising the steps of:

structuring functions necessary for processing a digital signal as a plurality of digital signal processing blocks and a host processing block, including at least a signal processing block for decoding and processing high speed streams of data, each of at least some of said digital signal processing blocks being operative to control hardware associated with said block ~~performing individual predetermined functions assigned thereto~~ by way of a hardware driver therein for driving the hardware associated with said block and having a processing unit for ~~supplying functionality instructions to activate~~ activating said hardware driver to control said associated hardware ~~of particular structure that is coupled to the block that performs said individual predetermined function, such that said hardware driver carries~~

~~out said predetermined function~~ in response to a high layer command supplied to said processing unit;

connecting the host processing block and the plurality of digital signal processing blocks through a common bus; and

outputting and transferring to the processing unit in a respective digital signal processing block, via said common bus, said high layer command, said high layer command being independent of the particular structure of the hardware coupled to said digital processing block, said high layer command being free of those functionality instructions that activate the hardware driver in said respective digital signal processing block to control the coupled hardware of particular structure, said high layer command being a general-purpose script type command that is interpreted by the processing unit in the digital signal processing block to which said high layer command is supplied to perform the function generally described by said high layer command, and said high layer command not being on a real time basis, said high layer command instructing the processing unit in said digital signal processing block to activate said hardware driver of said digital signal processing block to perform the predetermined function assigned to said respective digital signal processing block and;

supplying to said respective digital signal processing block, over said common bus, a high speed stream of data; and

wherein said processing unit of each of said digital signal processing blocks interprets and executes said high layer command to produce driver control instructions for said hardware driver to operate said hardware of particular structure ~~coupled to~~ associated with said digital signal processing block in accordance with said high layer command, and outputs said high speed stream of data.

14. (Previously Presented) The digital signal processing method as set forth in claim 13,

wherein the plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast, and

wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware.

15. - 17. (Canceled)

18. (Previously Presented) The digital signal processing method as set forth in claim 13,

wherein the high layer command is described and embedded in a script of hypertext.

19. (Previously Presented) The digital signal processing method as set forth in claim 13,

wherein the high speed streams of data contain video data and / or audio data.

20. (Original) The digital signal processing method as set forth in claim 19,

wherein the video data and / or the audio data has been compressed.

21. (Previously Presented) The digital signal processing method as set forth in claim 13,

wherein the bus is a general-purpose bus, and

wherein blocks can be added to said bus and a substitute for a connected block can be connected to said bus.

22. (Previously Presented) The digital signal processing method as set forth in claim 21,

wherein when a block is added or substituted, software for operating the added or substituted block is automatically installed.

23. (Original) The digital signal processing method as set forth in claim 21,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

24. (Previously Presented) The digital signal processing method as set forth in claim 21,

wherein when a block is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

25. (Currently Amended) The digital signal processing apparatus as set forth in claim 1,

wherein said host processing block has a high level interface for processing said high layer command; and

wherein each said plurality of digital signal processing blocks has a driver for interpreting said high layer command, and a low level interface for controlling said hardware.